

Attorney Docket No. 10559-393001
Application No. 09/823,276
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ABSTRACT

In one implementation, a programmable processor is adapted to include a first set of registers and a second set of registers. The first set of registers may have a future file, and the second set of registers may be architectural registers. Following a termination of an instruction in the processor, the future file may be restored with values in the second set of registers. The future file is restored over more than one clock cycle.